Place-and-Route for Photonic Integrated Circuits using Industry-Standard EDA Tools

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***Abstract*—Rapid advances of Electronic-Photonic Integrated Circuits (EPICs), across various material platforms, are driving the integration of thousands of photonic devices into complex heterogeneous systems. A key application is high-bandwidth communication for distributed computing. While manufacturing Photonic Integrated Circuits (PICs) leverages standard VLSI fabrication processes for electronic ICs, the PIC design ecosystem still lags behind the maturity of Electronic Design Automation (EDA) tools. To address this challenge, we introduce a publicly available, automated Photonic Place-and-Route (PnR) flow that operates across different material platforms and integrates seamlessly with industry-standard EDA tools. Our contributions include: (1) Photonic-to-electronic PnR mapping: Techniques to accommodate the distinct characteristics of photonic routing, such as waveguide bending constraints and optical metric mapping for performance optimization. (2) Comprehensive verification suite: A suite comprising Design Rule Check (DRC), Layout-vs-Schematic (LVS), and Parasitic Extraction (PEX) to ensure manufacturing compliance and accurate simulation using compact models (VerilogA/SPICE) of Electro-Optical devices. (3) Reference designs for multiple applications: Demonstrations include (a) high-bandwidth optical switch fabrics and (b) timing-optimized optical trees, that showcase the flexibility and performance of our Photonic PnR solution. For example: completing PnR of 1,000 devices in 20 & 50 minutes for timing-unconstrained & timing-constrained cases, respectively. This integrated approach enables more efficient design and optimization of EPICs, supporting future advances in electronic-photonic systems.**

***Index Terms*—Electronic-Photonic Integrated Circuits, EDA**

I. Introduction

Electronic-Photonic Integrated Circuits (EPICs) are advancing rapidly, with significant progress across multiple material platforms, including Silicon [1], Silicon Nitride [2], Thin-Film Lithium Niobate [3], Barium Titanate [4], and others [5]. In particular, the increasing demand for integrating increasing numbers of photonic devices is driving the development of heterogeneous systems with ultra-dense integration of electronics and photonics. Driving applications include high-bandwidth communication [6]–[9] and computing [10]–[12]. Despite the progress in manufacturing *Photonic Integrated Circuits (PICs: part of EPICs)*, which builds upon standard Very Large Scale Integration (VLSI) fabrication processes for electronic ICs, the *design ecosystem* for PICs still lags behind the more mature Electronic Design Automation (EDA) tools. Developing a cohesive EPIC design ecosystem is essential for co-design of electronics and photonics in heterogeneous EPICs.

Progress toward an EPIC design ecosystem includes the development of EPIC *Process Design Kits (PDKs)* [13], which include SPICE-compatible compact models for electro-optic (EO) devices (such as various EO modulators), and libraries of commonly-used cells (including schematic and layout representations). EPIC PDKs enable designers to simulate electronic and photonic circuit elements in a unified design and simulation environment (e.g., using Cadence Virtuoso), which is especially important for designing high-performance EPICs whose performance is limited by the interactions between electronics and photonics (such as overheads due to interconnect parasitics). However, as the number of photonic devices continues to grow, designers will increasingly rely on tools for *automated* design and verification of PICs, just as in standard EDA design flows for digital VLSI. A key part of the design flow, which we focus on in this paper, is placement-and-routing (PnR) of photonic ICs (i.e., photonic PnR). Essential characteristics of effective solutions for photonic PnR include:

- constraint-based optimization (e.g., timing constraints) [14],
- advanced routing optimization techniques (e.g., considering the curvature of photonic waveguides) [15],
- integration with industry-standard EDA tools (e.g., for electronic-photonic co-design of EPICs) [16].

While the cited works have made important contributions to photonic PnR, no single solution exhibits all of these characteristics simultaneously. In particular, the lack of integration with the broader *design automation toolchain* – including verification processes such as Design Rule Check (DRC), Layout-vs-Schematic (LVS), Parasitic Extraction (PEX), and EPIC performance simulation – limits their overall effectiveness.

In this paper, we present a publicly available, automated photonic PnR flow – comprising scripts, rulesets and example technology files – that leverages industry-standard EDA tools (Cadence Innovus and Siemens Calibre). Our photonic PnR flow, summarized in Figure 1, is material platform agnostic, and is seamlessly integrated with the broader EDA toolchain.

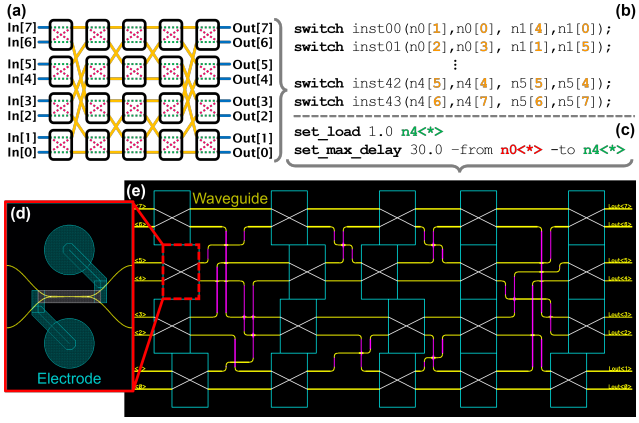

Fig. 1. Design process. The designer: (a) selects a topology (e.g., 8×8 Benes network [7]); (b) creates a netlist to define the interconnect; (c) sets the circuit performance constraints; (d) creates layouts for building blocks [17]; (e) generate the tapeout-ready physical design using photonic PnR.

Our key contributions are:

1) **Techniques for Mapping Photonic to Electronic PnR.** We demonstrate how to leverage industry-standard PnR for *electrical* circuits (Cadence Innovus) to perform *photonic* PnR (details in Sec. II). Our techniques account for fundamental differences in routing optical waveguides vs. electrical wires. For instance, waveguides typically have higher radius of curvature, and also can cross perpendicularly (on the same routing layer) with minimal loss and crosstalk. We also map desired optical metrics (e.g., loss or delay) to electrical wire delays (due to R and C), enabling Cadence Innovus to apply its mature optimization techniques to our photonic circuits (Sec. II-C).
2) **Comprehensive Verification Environment**, consisting of: (a) *Design Rule Check (DRC)*: ensuring the fabrication feasibility of the generated physical design by verifying compliance with manufacturing constraints; (b) *Layout-vs-Schematic (LVS)*: to validate correctness of the generated physical design – both schematics & layouts are developed in the OpenAccess standard and integrated with Cadence Virtuoso, enabling accurate analog simulations using VerilogA/SPICE compact models from EPIC PDKs; (c) *Parasitic Extraction (PEX)*: extracting the delays and crosstalk introduced by waveguide bends and crossings in the physical layout (Section III), producing picosecond-accurate models for simulation and optimization. Our full verification suite is described in Section IV.
3) **Reference Physical Designs for Multiple Applications** to demonstrate the effectiveness of our Photonic PnR flow (Sec. V). These include; (a) 128×128 Benes optical switch fabric designed for high-bandwidth, electrically controlled optical communication networks; and (b) a 1-to-16 Y-splitter tree, featuring unique delays per branch.

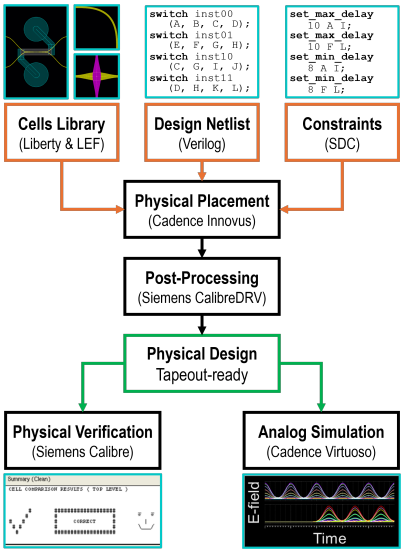

Fig. 2. Photonic PnR Design Flow. The designer supplies a cell library, a netlist, and performance constraints. These inputs, along with our open-source technology library, are processed by scripts implemented using industry standard tools as described in Figure 3 and generate a tapeout-ready physical layout. The flow concludes with physical verification in Siemens Calibre (DRC, LVS, PEX) and simulation in Cadence Virtuoso using the PEX netlist.

II. Photonic-to-Electronic Mapping

Figure 2 illustrates how we leverage mature PnR (for electrical ICs), verification & simulation EDA tools – long utilized in developing VLSI Electronic Integrated Circtuits (EICs) – for the automated design of EPICs. To accomplish this, we establish connections between the electrical and optical domains, identifying their similarities and differences, with the goal of describing optical properties in electrical terms that the tools can interpret.

The electrical and optical domains, particularly in their integrated circuit forms, share several similarities. First, optical waveguides and electrical wires exhibit similar geometric characteristics, such as rectangular or trapezoidal cross-sections and high length-to-width ratios (to connect separate components in an IC). Additionally, both serve as significant sources of delay in high-speed circuits – optical waveguides due to propagation delay in photonics, and electrical wires due to their characteristic RC constants in electronics. Finally, neither has inherent directionality, allowing both to be represented as directionless traces in a top-view layout.

Conversely, some of these commonalities diminish when considering the fundamental differences in propagation mechanisms. Optical waveguides cannot make sharp turns without significant losses, especially at 90° bends, whereas they benefit from maintaining directionality during interference, enabling the design of efficient waveguide crossings with low crosstalk and minimal losses, particularly when arranged perpendicularly. Additionally, the environment around electrical wires is highly capacitive due to isolating dielectrics, with multiple parasitic capacitances forming between neighboring wire segments, which deteriorates performance. In contrast, the precise coupling requirements of waveguides make unintended crosstalk a rare occurrence.

Together, these shared and unique properties establish a foundation for the following connections between the electrical and optical domains.

A. Propagation Delay

The first and primary connection between the optical and electrical domains regards the propagation delay of wires and waveguides. An RC network – a typical representation for a wire – exhibits a delay (Δt) given by:

$$\tau = R \cdot C \rightarrow \Delta t = \gamma \cdot \tau \tag{1}$$

where R is proportional to the length L of the wire, C is the terminating capacitance and γ is a scaling factor that varies depending on the tool and the definition of the delay (e.g., $\ln 2$ for a 50% rise time). Similarly, the phase delay of a waveguide is calculated as:

$$\Delta t = \frac{L}{c_0 / n_{eff}} \tag{2}$$

where c_0 is the speed of light in vacuum and n_{eff} is the effective refractive index of a specific waveguide mode and wavelength.

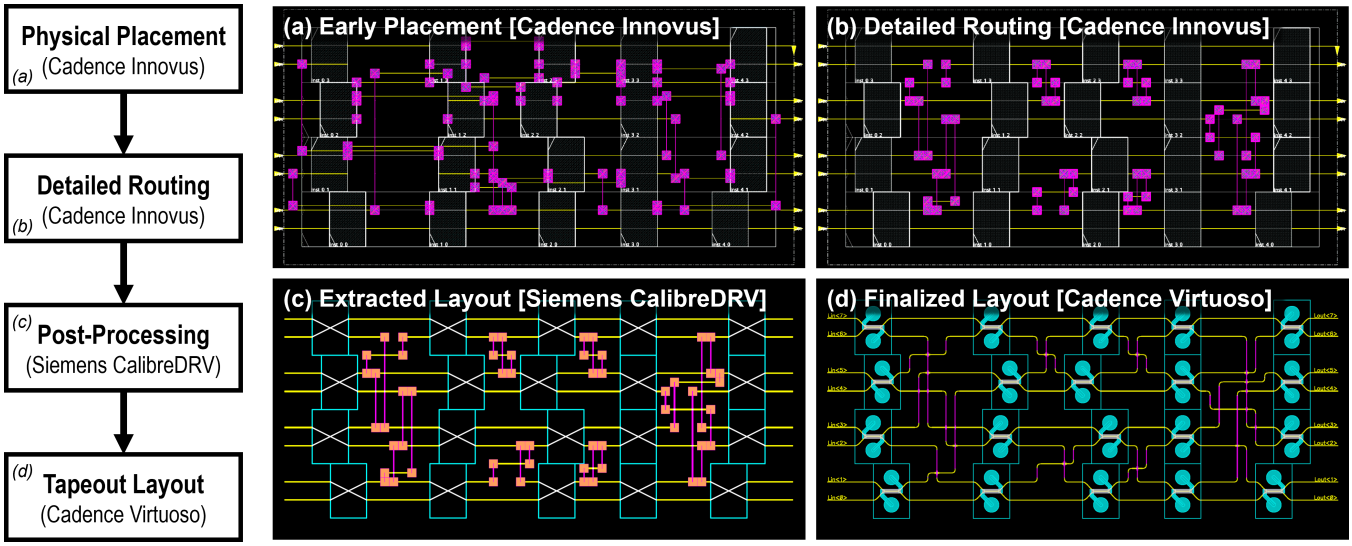

Fig. 3. Physical Implementation Steps. (a) Initial placement and (b) detailed Routing are performed in Cadence Innovus using standard command scripts with additional restrictions for photonic routing (e.g., coarse grid, enforcing 1D routing) – Section II-A – and performance constraints – Section II-C. Next, (c) post-processing in Siemens CalibreDRV replaces sharp corners with bends and defines crossing points – Section III – to (d) produce a tapeout-ready physical layout, integrating the building blocks defined in Cadence Virtuoso.

Combining those equations to create a "bridge" between the delay wire/waveguide hybrid (defined as *wireguide*), we end up with an electro-optical formula:

$$\begin{aligned} \gamma \cdot R(L,W) \cdot C &= \frac{L}{c_0/n_{eff}} \\ \xRightarrow{\text{fixed } W} \gamma \cdot R(L) \cdot C &= \frac{L}{c_0/n_{eff}} \\ \Rightarrow R(L) &= n_{eff}\,\frac{L}{\gamma \cdot C \cdot c_0} \end{aligned} \tag{3}$$

where $R(L)$ is the per-length resistance, a commonly used property in EDA tools for the characterization of conductors.

Equation 3 enables us to calculate the effective delay of a varying-length wireguide by setting the terminating capacitance to a fixed value, e.g. 1pF. This ensures that the in-series resistance of the wireguide is proportional to its length, and consequently, the propagation delay is also proportional to length, as expected for a waveguide. For example, we calculate R of a 1µm-wide, 100µm-long waveguide as 330mΩ for $n_{eff} = 1$, while γ was tuned to 0.6564 for Cadence Innovus.

A similar approach can be used to calculate optical losses within the routing of the design

$$R(L) = \frac{\alpha \cdot L}{\gamma \cdot C} \tag{4}$$

with α is the waveguide loss coefficient in dB/µm. The report from the PnR tools references it as time, but the actual values will represent loss in logarithmic scale.

Another significant advantage of this methodology is that the technology node characterization files, known as TechLEF – which contain resistance and capacitance information of wireguides and are used by PnR tools to calculate wireguide propagation delays – can be generated once with $n_{eff} = 1$, using Cadence Quantus, and subsequently scaled using a resistivity scaling factor to match the desired refractive index and the smallest possible capacitance scaling to minimize the contribution of the wireguides to the fixed load capacitance.

B. Routing Restrictions

We next discuss the characteristics and imposed restrictions in the technology file that enable the use of electronic PnR tools for photonic routing, as illustrated in Figure 4.

Beginning with the layer definition, we represent an optical waveguide as a metal nano-wire within the PnR tools. While most PIC platforms support only a single waveguide routing layer, the concept of low-loss, low-crosstalk single-layer crossings that exists in photonics is absent in electronics. To address this, we establish two separate routing layers: one exclusively horizontal and one exclusively vertical, a routing method also identified by [18] (recently enabled by strict routing capability in Cadence Innovus).

This dual-layer approach enables EDA tools to comprehend different signals in these distinct orientations, while intersections can be easily identified and be materialized as waveguide crossings with minimal interference and losses. Furthermore, this perpendicular-orientations technique helps reduce waveguide losses associated with electron beam lithography, an advantage particularly useful in low-volume fabrication settings, such as academic cleanrooms, as noted by [19].

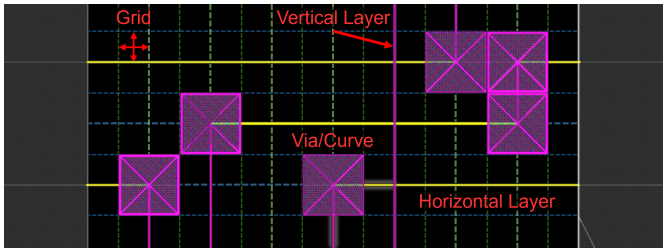

Fig. 4. Waveguide Routing. Routing is implemented in a standard EDA PnR tool (Cadence Innovus) with stringent constraints. "Wiring" is restricted to two "layers" – one horizontal and one vertical – with strictly enforced direction (1D routing). Oversized vias enable continuity between "layers" and provide sufficient space for subsequent curve replacement. The curve dimensions also define the coarse routing grid.

Another key factor to consider is the manufacturing grid, which determines where waveguides can be positioned within the layout. We employ a coarse grid with a spacing around $10\mu m$ for two main reasons. Firstly, recent advances in low-loss adiabatic bends across most PIC material platforms have achieved bend radii within this range [20], [21]. Secondly, since parallel waveguide coupling is a primary source of crosstalk in PICs, this spacing provides sufficient isolation between waveguides, even over extended distances [22]. Together, these factors make a coarse grid approach an effective solution, but also enables flexibility because the dimensions of it can be fine-tuned for different technologies.

The final element required to achieve full routing capabilities with an industry-standard PnR tool is the via definition. Here, we use vias as objects to enable intentional orientation changes for specific signals, physically implemented using the previously discussed low-loss bends. The via dimensions are based on the size of these bends and must fit between non-adjacent grid lines. Specifically, the via width is defined as:

$$\text{width}_{via} = 2 \times \text{radius}_{bend}$$

and allows any possible orientation change for bends, in post-processing, without interfering with adjacent waveguides.

We use all these techniques to develop the open-source technology libraries, configuration files and scripts for Cadence Innovus and manage to place (Figure 3a) and route (Figure 3b) the design. Additionally, the generality of our approach and use of widely adopted formats facilitate adaptation to other, similar EDA tools (e.g., Synopsys Design Compiler).

C. Optimization

With the basic principles of mapping optical properties to electrical counterparts and defining photonic routing restrictions, we can now leverage the mature algorithms of PnR tools to measure (Figure 5) and perform constraint-based optimization (Figure 6) of our design according to timing or loss specifications. The structure and operation of photonic circuits closely resemble those of combinatorial electronic circuits, allowing us to apply many relevant optimization techniques. A commonly used constraint is *set_max_delay*, defined in the Synopsys Design Constraints (SDC) format, which effectively limits the maximum routing length between specified points/signals, thereby driving the optimization of placement and routing, as seen in Figure 3b.

Along with setting an upper limit on propagation delay, it can also establish a minimum delay for timing-sensitive applications. This is achieved using the *set_min_delay* command, which ensures that signals reach their destination after a specificied time. In manual implementations, this could be achieved with waveguide spirals [23], but PnR tools cannot directly interpret or implement this concept. Therefore, designers need to create delay cells that apply these techniques and can be used during optimization to align path timing based on the constraints. For our case-study applications (Section V), we designed simple delay cells (Figure 6) to meet the requirements, but advanced geometries can be utilized too.

```
#####################################################################
#  Generated by:       Cadence Innovus
#  OS:                 Linux x86_64
#  Command:            report_timing
#####################################################################
Path 1: Unconstrained input
Endpoint:   Lout[3]
Beginpoint: Lin[0]
Analysis View: av_typical
Arrival Time:  26.400
+-------------------------------------------------------------------------------------------------+
| Instance |   Arc    |  Cell  |  Instance Location |    Net    |  Load | Delay | Arrival |
|          |          |        |                   |           |       |       |  Time   |
|----------+----------+--------+-------------------+-----------+-------+-------+---------|
|          | Lin[0]   |        |                   | Lin[0]    | 1.004 |       |   0.000 |
| inst_0_0 | Lc -> Lb | switch | (250.00, 100.00)  | nets1[4]  | 1.021 | 3.000 |   3.000 |
| inst_1_2 | Lc -> Lb | switch | (900.00, 700.00)  | nets2[6]  | 1.011 | 7.500 |  10.500 |
| inst_2_3 | La -> Lb | switch | (1400.00, 1000.00)| nets3[5]  | 1.013 | 2.500 |  13.000 |
| inst_3_2 | La -> Ld | switch | (1850.00, 700.00) | nets4[2]  | 1.017 | 4.800 |  17.800 |
| inst_4_1 | La -> Ld | switch | (2450.00, 400.00) | Lout[3]   | 1.003 | 7.200 |  25.000 |
|          | Lout[3]  |        |                   |           | 1.003 | 1.400 |  26.400 |
+-------------------------------------------------------------------------------------------------+
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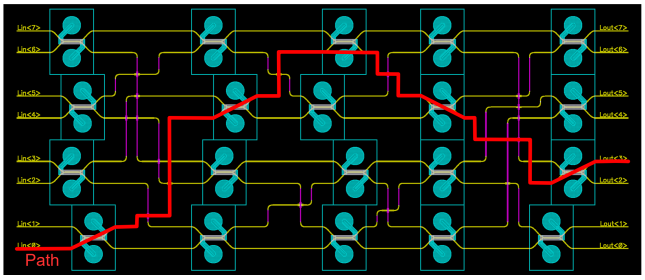

Fig. 5. Timing Report. The report from Cadence Innovus details each segment of the optical path from input to outputs across the network. It calculates a path delay of 26.4 ps for this specific route, while a manual estimate based on path length and waveguide refractive index approximates 27 ps. The fixed termination load (~1 pF) on each net allows accurate calculation of propagation delay for each routing segment, with small variations resulting from the non-zero capacitance of the wires (required by Cadence Innovus).

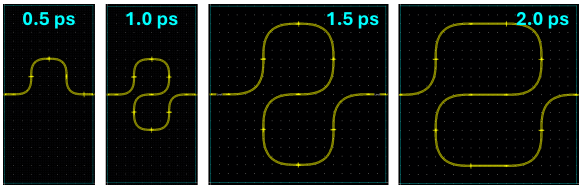

Fig. 6. Delay Cells. Timing optimization in PnR tools relies on delay cells (buffers in electronics). Optical delay cells were designed with varying delays by incorporating waveguide bends to increase propagation delay.

III. Layout Post-processing

This section focuses on the post-routing steps that transform the placed-and-routed design (Figure 3c) into a high-performance, tapeout-ready layout (Figure 3d). As shown in Figure 7, two key operations are required: substituting vias with tuned bends and defining optimized crossings at perpendicular waveguide intersections. We execute both tasks using automated scripts implemented in CalibreDRV, relying solely on standard layout manipulation commands.

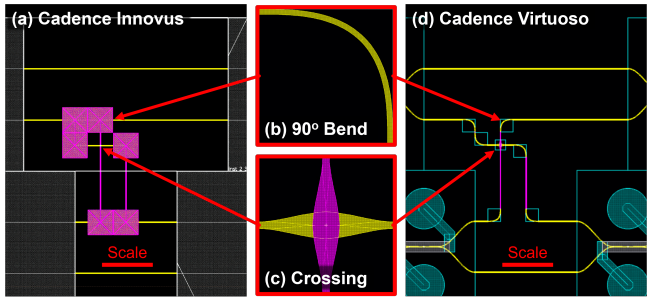

Fig. 7. Layout Post-processing. Utilizing an automated script in Siemens CalibreDRV, (a) the layout generated is processed. (b) Vias are replaced by appropriately oriented bends. and (c) intersections between the two "layers" are detected and replaced with optimized waveguide crossings to minimize losses and crosstalk. (d) The final layout is tapeout-ready.

Bend locations are identified by the origins of the vias in the exported layout, though the orientation is initially undetermined. Orientation is established by analyzing the waveguide segments within each via rectangle and their relative positions (left/right for the horizontal layer and top/bottom for the vertical layer). Once this relative positioning is determined, we place the appropriate tuned bend cell reference and repeat the process for each subsequent bend. Additionally, we identify all intersection areas of the two layers (horizontal and vertical) as rectangles and replace each intersection with a waveguide crossing, centered within the rectangle. These modifications result in a layout that adheres to fabrication rules & tolerances and complies with all optical domain peculiarities.

IV. Verification

Here, we discuss how integration with a standard EDA toolchain – particularly verification – is achieved, enhancing our flow's capabilities and expanding the range of tools available to the designer, such as fabrication rule checking, implementation validation and analog simulation.

Starting with Design Rule Checking (DRC), an essential tool for verifying design feasibility and often identifying layout errors, we establish a set of rules to ensure fabrication tolerances (e.g., spacing between short waveguides), detect incorrect shapes (e.g., sharp corners), and maintain signal integrity (e.g., spacing between long waveguides).

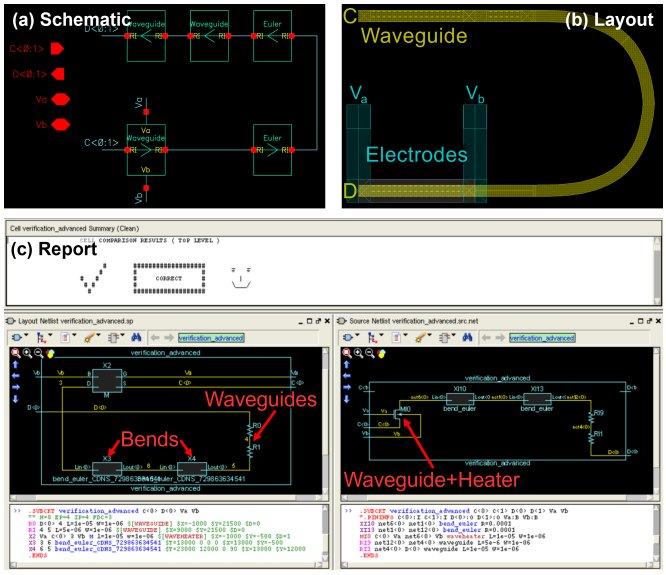

Fig. 8. Layout vs. Schematic (LVS). (a) Schematic is compared with (b) layout, both created in Cadence Virtuoso using an Electro-Photonic PDK. (c) This Siemens Calibre screenshot demonstrates successful LVS verification, where our rule deck identifies waveguides as resistors, waveguides with heaters as transistors, and treats other components as black boxes.

In Figure 8, we illustrate an example of our Layout vs. Schematic (LVS) procedure – a key component of the verification suite – implemented and executed in Siemens Calibre. Applying methodologies similar to electronic LVS, we identify waveguides as rectangles within the designated layer, measure their dimensions, and interpret them as simple, non-directional two-terminal devices, such as resistors. Similarly, when a waveguide includes an integrated heater, we model it as a four-terminal device, akin to a transistor, with the source/drain carrying the optical signal and the gate/body handling the electrical signals. We treat temaining building blocks – such as crosses, bends, and custom cells – as black boxes, where only their interconnections with other components are analyzed, and internal layout details are not processed.

With both DRC and LVS procedures in place, we build upon the concepts described in the LVS paragraph to form the PEX ruleset, enabling the extraction of unrecognized routing segments as waveguides, as illustrated in Figure 9. This step is critical in an automated PnR flow implemented on EDA tools, as nano-wires are typically not primary delay sources in electronic circuits but waveguides can be photonic circuits. Consequently, routing segments are transferred between tools as ideal shorts, resulting in a loss of the inherent delays. In this procedure, we identify each straight routing segment, bend & crossing, creating an equivalent PEX netlist ready for detailed analog simulation with any EPIC PDK equipped with VerilogA/SPICE models.

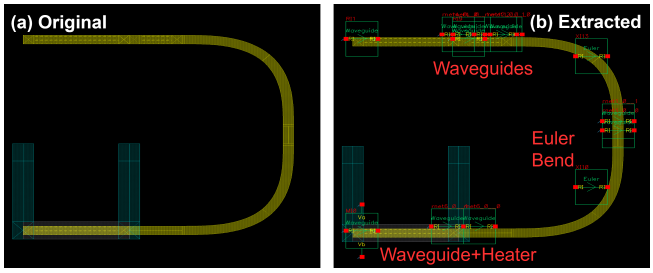

Fig. 9. Parasitic Extraction (PEX). (a) The layout undergoes Parasitic Extraction in Siemens Calibre, where waveguides and waveguides with heaters are identified as fundamental devices, while other components are treated as black boxes. (b) The resulting netlist, modified via post-processing scripts, is ready for analog simulation using the Electro-Photonic PDK.

A fine detail that arises in post-PEX simulation is that photonic devices are primarily described using invertible transmission matrices, a concept not supported by VerilogA and SPICE models. Consequently, photonic models implemented in EPIC PDK using these EDA standards require inherent directionality, with designated input and output ports. This requirement conflicts with our PEX procedure, as the resistors and transistors used as mapped devices for waveguides employ linear transfer functions and are inherently bi-directional. To address this, we process the resulting netlist, using a script in Cadence Virtuoso, starting from the designated inputs of the design and traversing through each device to check and adjust its orientation until we reach a designated output as shown in Figure 10.

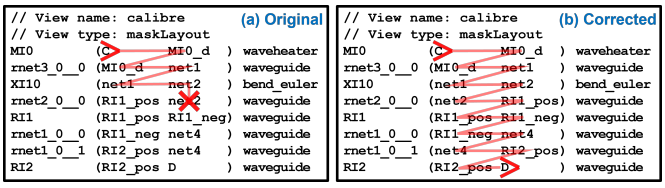

Fig. 10. Netlist Processing. Some VerilogA and SPICE electro-photonic models have specific directionality. An automated script in Cadence Virtuoso processes (a) the original PEX netlist to verify and adjust device orientation along each path and (b) generates the final simulation-compatible netlist.

V. Reference Designs and Applications

This section includes the design and evaluation results of reference designs using our Photonic PnR flow for high-radix optical switch fabric using the Benes network topology (Figure 11) and timing optimized Y-splitter tree (Figure 12).

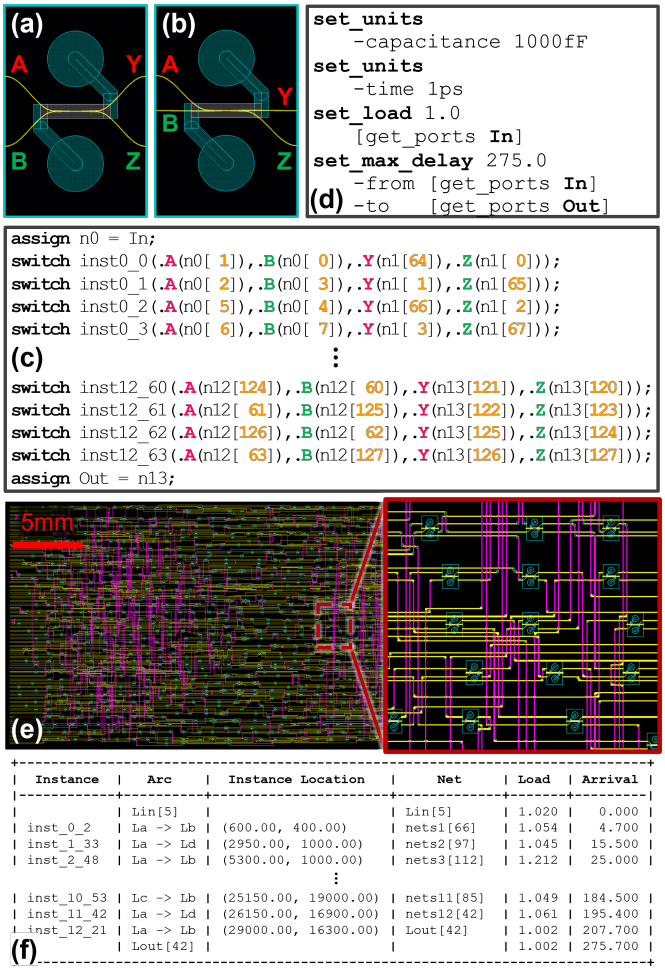

Fig. 11. Example Application (A). A 128x128 Benes Network implemented with our Photonic PnR flow. (a) The initial symmetrical cell was replaced by (b) an asymmetrical version to minimize DRC errors. Using (c) the Verilog definition of the network and (d) corresponding performance constraints, we perform automatic place-and-route – in *40 minutes* – resulting in (e) a final layout and (f) a timing report confirming compliance with specifications.

Expanding from a low-radix network (Fig. 1) to a high-radix one (Application A, Fig. 11), the symmetrical 2x2 switch caused routing issues in Cadence Innovus, resulting in hundreds of DRC errors due to port alignment. Slight port asymmetry resolved these errors originated in crossed routing between neighbouring cells.

TABLE I
Comparison with State-of-the-Art Photonic IC Place-and-Route Tools

	This work	PROTON'13 [14]	ADEPT [12], [15]	Autorouting [16]
Cell Placement	Yes	Yes	No	No
Advanced Routing	Potential Upgrade	No	Yes	No
Electrical Routing		No	No	Automated
Tool Integration	Full	None	None	Full
Publicly Available	Yes	Yes	Yes	No
Special License	No	Not applicable		Yes

In another case, we aim to achieve precise & distinct propagation delays across branches in an equi-power optical binary tree (Fig 12). As output count increases, we apply lower & upper timing constraints need to meet the desired delays.

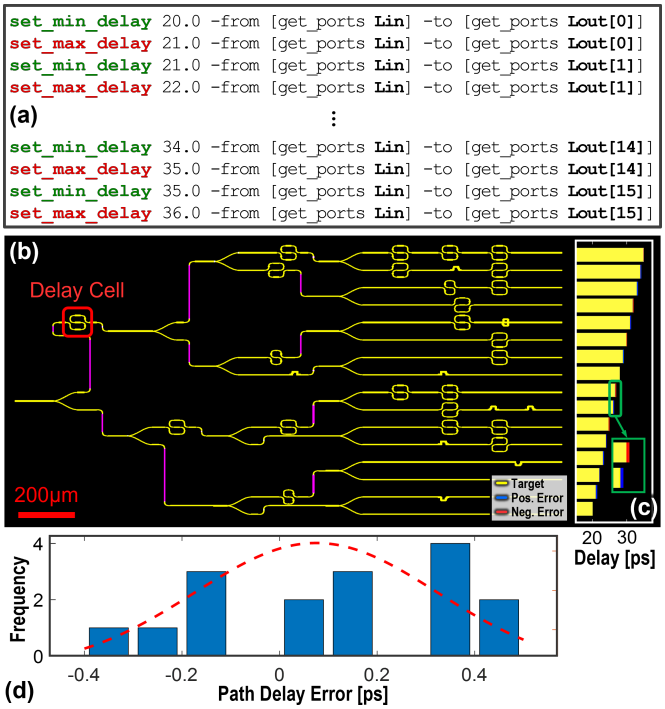

Fig. 12. Example Application (B). A 16-output binary tree using Y-splitters and delay cells to achieve varied branch delays. (a) Constraints defined in SDC specify desired propagation delay from input to each output, (b) yielding a layout in under *2 minutes*. (c) Optimization targets these constraints (yellow), with error shown as positive (blue) or negative (red). (d) Errors are distributed around zero, with a maximum of <2% and an average of ~1%.

VI. Conclusion

By leveraging today's mature EDA tool ecosystem for EPICs, designers can capitalize on decades of infrastructure development to enhance both system performance and the efficiency of the design process. This is in stark contrast to reinventing design automation tools for PICs from the ground up. Accordingly, this paper provides the foundations for meeting the unique needs of PIC and EPIC-based heterogeneous systems, by adapting *existing* PnR and physical verification EDA tools. To do so, we present techniques for mapping optical properties to electrical equivalents for performance characterization, and for physical verification of EPICs in within a unified design flow. We also provide example technology files and reference designs to kickstart the adoption of these techniques by larger design communities. Areas for continued development include enhanced modeling of delay and loss due to waveguide crossings and bends, advanced routing techniques for higher EO device density, and simultaneous routing of electrical circuits and photonic circuits to minimize interconnect overheads. Using this work as a stepping stone, design communities can continue integrating electronic-photonic design considerations into existing EDA methodologies, to build a comprehensive development toolchain for heterogeneous EPICs as they continue to evolve.

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